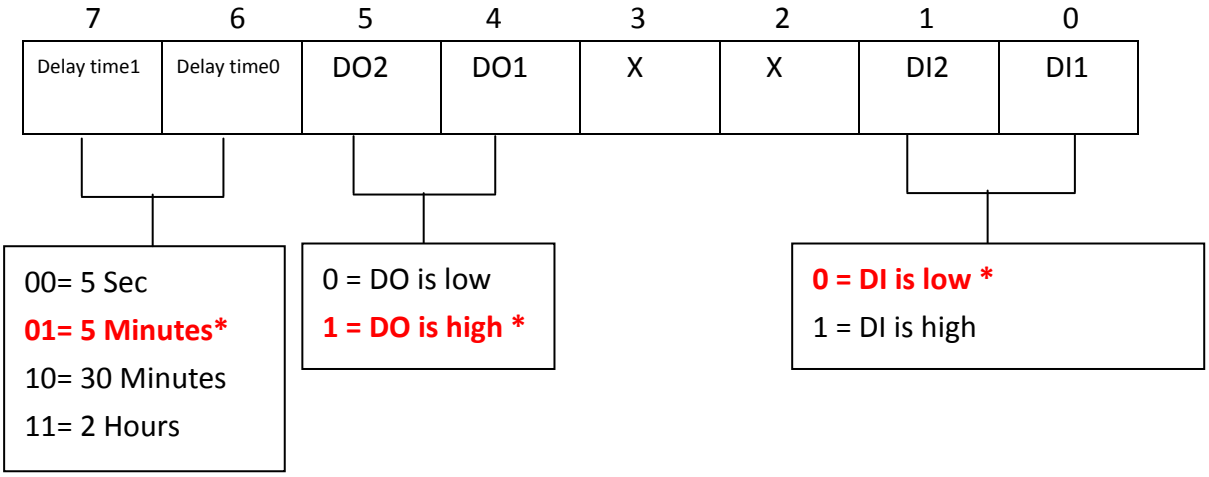
GPIO & Delay Time & Ignition & 3G Reset Setting

1. GPIO and Delay Time Control Register

The General Purpose I/O is an interface available on some devices. These can read digital signals from other parts of a circuit, or output to control other devices. At GPIO control register, the GPI is use to receive data, the GPO is set data to send.

I/O port: Read A2h / Write A1h



GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Default	Description
7	GPIO57_OE	R/W	0	0: GPIO57 is input. 1: GPIO57 is output.
6	GPIO56_OE	R/W	0	0: GPIO56 is input. 1: GPIO56 is output.
5	GPIO55_OE	R/W	0	0: GPIO55 is input. 1: GPIO55 is output.
4	GPIO54_OE	R/W	0	0: GPIO54 is input. 1: GPIO54 is output.
3	GPIO53_OE	R/W	0	0: GPIO53 is input. 1: GPIO53 is output.
2	GPIO52_OE	R/W	0	0: GPIO52 is input. 1: GPIO52 is output.
1	GPIO51_OE	R/W	0	0: GPIO51 is input. 1: GPIO51 is output.
0	GPIO50_OE	R/W	0	0: GPIO50 is input. 1: GPIO50 is output.

GPIO5 Output Data Register — Index A1h

Bit	Name	R/W	Default	Description
7	GPIO57_DATA	R/W	1	GPIO57 output data in output mode.
6	GPIO56_DATA	R/W	1	GPIO56 output data in output mode.
5	GPIO55_DATA	R/W	1	GPIO55 output data in output mode.
4	GPIO54_DATA	R/W	1	GPIO54 output data in output mode.
3	GPIO53_DATA	R/W	1	GPIO53 output data in output mode.
2	GPIO52_DATA	R/W	1	GPIO52 output data in output mode.
1	GPIO51_DATA	R/W	1	GPIO51 output data in output mode.
0	GPIO50_DATA	R/W	1	GPIO50 output data in output mode.

GPIO5 Pin Status Register — Index A2h

Bit	Name	R/W	Default	Description
7	GPIO57_ST	R	1	GPIO57 pin status.
6	GPIO56_ST	R	1	GPIO56 pin status.
5	GPIO55_ST	R	1	GPIO55 pin status.
4	GPIO54_ST	R	1	GPIO54 pin status.
3	GPIO53_ST	R	1	GPIO53 pin status.
2	GPIO52_ST	R	1	GPIO52 pin status.
1	GPIO51_ST	R	1	GPIO51 pin status.
0	GPIO50_ST	R	1	GPIO50 pin status.

GPIO5 Drive Enable Register — Index A3h

Bit	Name	R/W	Default	Description
7	GPIO57_DRV_EN	R/W	0	GPIO57 Drive Enable. 0: GPIO57 is open drain. 1: GPIO57 is push pull.
6	GPIO56_DRV_EN	R/W	0	GPIO56 Drive Enable. 0: GPIO56 is open drain. 1: GPIO56 is push pull.
5	GPIO55_DRV_EN	R/w	0	GPIO55 Drive Enable. 0: GPIO55 is open drain. 1: GPIO55 is push pull.
4	GPIO54_DRV_EN	R/W	0	GPIO54 Drive Enable. 0: GPIO54 is open drain. 1: GPIO54 is push pull.
3	GPIO53_DRV_EN	R/W	0	GPIO53 Drive Enable. 0: GPIO53 is open drain. 1: GPIO53 is push pull.
2	GPIO52_DRV_EN	R/W	0	GPIO52 Drive Enable. 0: GPIO52 is open drain. 1: GPIO52 is push pull.
1	GPIO51_DRV_EN	R/W	0	GPIO51 Drive Enable. 0: GPIO51 is open drain. 1: GPIO51 is push pull.
0	GPIO50_DRV_EN	R/W	0	GPIO50 Drive Enable. 0: GPIO50 is open drain. 1: GPIO50 is push pull.

I/O port: Read F2h / Write F1h

I/O port: F2h

7	6	5	4	3	2	1	0
X	X	X	X	Ignition Status	X	X	X

0 = Ignition off
1 = Ignition on

I/O port: F1h

7	6	5	4	3	2	1	0
X	X	X	X	X	3G Reset	X	X

0 = Keep Low 2 Sec → 3G Reset
1 = Modem Normal Operating

2. WDT Setting

I/O port: **A10** (base address) + 05h and 06h

0xA15 → Value for watchdog

0xA16 → Command execution : 0x32 for sec and 0x3A for Minutes.

2.1 Watchdog Timer Control Register

The Watchdog Timer Control Register controls the WDT working mode. Write the value to the WDT Configuration Port. The following table describes the Control Register bit definition:

7	6	5	4	3	2	1	0
0	0	1	1	Timer Unit	0	Select output pulse width of RSTOUT#	

0 = 1 sec
1 = 60 sec *

00 = 1 ms
01 = 25 ms
10 = 125 ms*
11 = 5 sec

O A16 05

O A15 32 // 5 sec // 3A → 5 minutes

7.9. Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting.

The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Others, please refer the device register description as below.

Watchdog Timer Configuration Register 1— base address + 05h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.

5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — base address + 06h

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	Time of watchdog timer

Watchdog PME Control Register — base address + 0Ah

Bit	Name	R/W	Default	Description
7	WDT_PME	R	--	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5-1	Reserved	--	--	Reserved.
0	WDOUT_EN	R/W	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.